dCS Control Board v7

Service Manual

October 2009

[1] ***dCS*** is Data Conversion Systems Ltd. Company registered in England No. 2072115.

Contents

SAFETY AND CONFIDENTIALITY

Safety Warnings

Servicing must be carried out by qualified service personnel only.

These products contain circuitry that operate at high voltages and/or currents. Removing safety covers can expose personnel to risk of electric shock or other injury.

Take special care when working on the Power Board, as much of the board is at high voltage.

These products contain static-sensitive devices which can be seriously damaged by incorrect handling. Observe standard anti-static precautions at all times.

This product is lead-free to comply with the RoHS directive. If soldering or de-soldering is required, SAC solder (tin / silver / copper) must be used to ensure reliable repairs.

Always use genuine replacement parts supplied by ***dCS***.

Disclaimer

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Confidentiality

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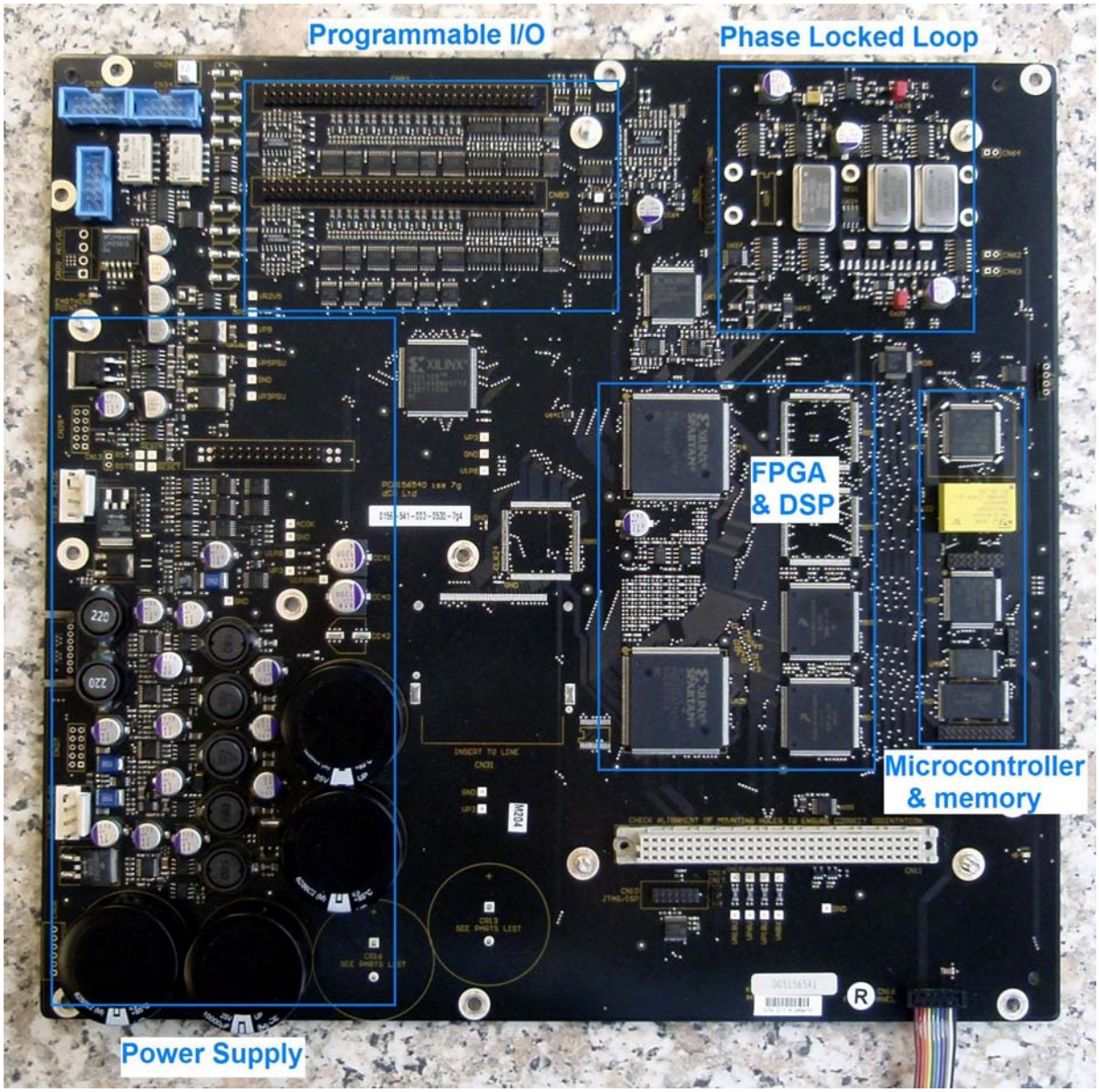
ASSEMBLY DESCRIPTION



The v7 Control Board DCS156541 forms the digital processing platform for nearly all current dCS products: the Scarlatti and Paganini series plus the Puccini Player.
As shown in the photo above, the circuitry is divided into the following sections.

Power Supply

The Control Board may be supplied from one or two low-voltage mains transformers connected to CN17 and/or CN18. The low-voltage AC supply is converted to nominally 12V DC by D102/CR11-13 and D104/CR14-16, which drive a group of DC-DC converter circuits to generate the main DC rails. Two transformers are used on Scarlatti DACs and the snap-off tab between CN17 & CN18 is removed to separate the analogue and digital supplies. One transformer is fitted to most products, connected to either CN17 or CN18, and the tab is left in place.

The -POFF line connects from the Display to the Control Board via CN16 and then to the Power Board via CN19. With power connected but the unit switched off, a small DC current injected from the Power Board keeps -POFF around +0.5V. Pressing the Power Button shorts -POFF to ground, which turns the Power Board on and energises the mains transformer(s). Linear regulators U109 & U120 generate the VP5PSU (+5V) and VP3PSU (+3.3V) rails from the 12V DC rail. These two rails plus VP12C power circuitry that must be active before the main supplies are available.

Dual comparators U116/117 generate two “PSU TICK” 100/120Hz pulse trains and drive the “ACOK” line high when the incoming AC is present - these give an early warning to the microcontroller (once it has booted up) if the supply is turned off or disconnected or fails.

U213 generates a reset by pulling -VP3PSURST low, latches U112/5 & /9 are reset, U107/11 drives the ON line high, starting up the DC-DC converters: U201 (VP3), U203 (V1P8), U212 (VP6), U216 (VN8) and U301 (VP18). Linear regulators generate other lower voltage rails: U204 (VP5, U202 (VN5), U303 (VP9) and U305 (VR2V5). While the ON line is low, VP12B is disconnected from VP18/VN18 DC-DC converters U301/U302 by U307/TR33. U302 is controlled directly from the micro via the -VN18EN line, it is activated only on DACs at present. Watchdog chips U213, U214 & U209 monitor the VP3PSU, VP3 & VP5 rails, they issue a reset command if the voltage on any of these rails drops too low.

(There is provision for an external 12V DC supply to be connected via CN17/18 pins 3/2 – this is not used on current consumer products. The main power supplies are turned on via U111 and TR16/D103/D105. U110 monitors the incoming DC and drives the “DCOK” line high.)

After boot-up, the unit can be set to Sleep mode by pressing the POWER button briefly. All power supplies continue running, but the micro disables some functions (the main display is turned off, front panel controls other than the POWER button are disabled, outputs are muted).

From normal operating mode, if the POWER button is held down for a few seconds, Power Down appears on the display. When the POWER button is released, the micro drives the OFF A line high and the OFF B line low, which turns the Power Board off, disconnecting power from the mains transformer(s). U219/4 turns on transistors TR23-24, TR26-28, which help discharge the VP6U, VP5, VP3, V1P8 and VP18U rails.

Microcontroller & Memory

This section consists of a 16-bit microcontroller U402, memory mapper CPLD U407, 512kB SRAM U406, 4MB flash memory U405 and battery backed-up 32kB SRAM with real-time clock U403. The microcontroller and memory chips are interconnected by address bus UA[0:23] and data bus UD[0:7]. Selection of the memory chips is controlled by the microcontroller via chip select bus –CS[0:4] and the CPLD. The functionality of the board is controlled by firmware stored in the flash memory. New software may be loaded from a small programmer board (which fits on 3 headers over U405-407) or (in most cases) from the outside of the box from an update CD-R.

In normal use, the back-up battery for U403 will last for several years, depending on temperature and what proportion of the time the unit is switched completely off.
Do not remove the yellow battery pack for any reason while the unit is switched off, as the data stored in U403 (such as clock calibration data) will be permanently erased.

The micro drives a red diagnostic LED D401, which gives a crude indication of activity. Serial debug port CN12 provides a detailed log of micro activity which may be viewed on a PC – see page **13**.

The microcontroller is used for set-up and supervisory functions, it is not used for time-critical operations or audio processing.

FPGA & DSP

The signal processing and decoding functions are carried out by FPGA U505 and DSP chips U503 & U504. There is provision for 2 more DSP chips in locations U501 & U502, but these are not fitted on the “audiophile” version of the Control Board. Another large FPGA U718 performs the PLL and clocking selection functions. Clock multiplication for the FPGAs is performed by PLL chips U606 & U607.

During boot-up, configuration data is loaded from flash memory into FPGAs U505 & U718 via the CCLK, DONE, -INIT & -PGRM lines from the micro. The DONE line goes high when loading is complete. The FPGA configuration does not change again until the board powers down. DSP code is loaded from flash memory into DSPs U503 & U504 via the micro and U505. Different DSP code is loaded each time the sample rate changes.

During boot-up, the V1P8 rail is turned on, the V1P8GD line goes high, the outputs of dual comparator U508 go high and dual MOSFET TR55 turns on, connecting power to the FPGAs (VP3B & V1P8B). This ensures the FPGAs power up in a controlled manner.

Phase Locked Loop (PLL) & Clock Generator

The clock generator either generates a stable clock when the unit is operating in master mode, or synchronises one of the voltage-controlled crystal oscillators (VCXOs – X01 or X02) to an incoming clock signal. X01 (24.576MHz) is selected if the sample rate is related to 48kHz, X02 (22.5792MHz) is selected if the sample rate is related to 44.1kHz. Transports and Players fitted with an Esoteric CD mechanism have a 27MHz crystal fitted in the X03 position, this is used by the Esoteric electronics only. A red LED near each crystal illuminates when that crystal is active. The whole board powers up on X02 and then runs from either X01 or X02 depending on the data rate.

Operation of the PLLs and Clocks is controlled by CPLD U619 and FPGA U718. All of the available audio and clock sources on IOLINK[23:0] are connected to the inputs of analogue selector chips U646, U647 & U649. Input selector bus ISEL[5:0], which is generated by the FPGA, connects one of the sources to the output, the signal is buffered by U648 and the output ICLOCK is passed to the FPGA.

A variety of frequency control signals can be routed to the control ports for the 4 VCXOs X01-4 via 4 analogue selector chips U612, U614, U616 & U618. The selectors are driven from U619 via bus CSEL[11:0], which allows each VCXO to be controlled from a different source, these are:

- VCS0 - the output of the primary PLL, used for locking to a source.
- VCS1 – the output of the secondary PLL, used to lock a second VCXO to the main one.
- GND – sets the frequency to minimum (<-300ppm).
- VP5VCO – the low noise +5V VCXO supply, sets the frequency to maximum (>+300ppm).
- VR2V5 - sets the VCXO frequency close to centre (perhaps +/-20ppm).
- EXT1 – provision for an external feed via CN64.

Low noise rails for the clock circuitry are generated by U628/1 & TR61-63 (+5V – VP5VCO) and U628/7 & TR64-66 (+3.3V – VP3CLK). The VCXOs are powered individually from VP5VCO by TR51-54 under control of CPLD U619 via U630-633 and the -ON[3:0] bus. Each VCXO has a nearby red LED D402-405 to indicate that it is active. VCXOs are turned off to reduce interference when not needed. The VCXO outputs are connected back into U619 via U627, and also feed the inputs of 3 analogue selector chips U613, U615, U617. The selectors are driven from U619 via bus VSEL[8:0], allowing main clocks CLK24, CLK24A and CLK22 to be driven from any VCXO.

When the board is locking to an external source, the main PLL operates as follows. The selected data stream ICLOCK is applied to a phase detector in the FPGA and compared to the output of the relevant VCXO. The resulting pulse train appears on one of the PDO[3:0] lines (depending on the time constant required – usually PD0[1]) which drives integrator U657 and 16-bit ADC U642. The ADC data (ADCD) is passed back to the FPGA, which digitally filters the data, noise shapes it and truncates to 1-bit. DACOP is re-clocked by latch U602/4, filtered by U602 and routed to the selected VCXO's control port, completing the loop.

When the board is generating the master clock for the system, the FPGA drives noise shaped data directly to the DACOP line, which is again re-clocked, filtered and drives the selected VCXO. The 1-bit data is generated from the individual crystal calibration data. Single-temperature calibration is used for Players, Transports and DACs, while the more intensive calibration procedure used for Master Clocks corrects for crystal drift over a substantial temperature range (+10 to +40°C). The temperature sensor U624 is located near the VCXOs, its output is routed to FPGA U718. If the sensor detects an excessive temperature, it commands the microcontroller to shut the board down.

The secondary PLL is much simpler, it is usually used to lock 2 VCXOs together (in a Master Clock or Upsampler). The two crystal outputs are compared by a second FPGA phase detector. The resulting pulse train appears on one of the PD1[3:0] lines (depending on the time constant required – usually PD1[0]) which drives integrator U629/8. Switch U645/4 selects either fast settling mode or fine lock mode, it is typically used in the fast settling mode. The output is routed to the secondary VCXO's control port.

When either operating in Master Mode or locked to an accurately-calibrated source, the DC voltage on the control port (pin 1) of the primary VCXO should be very close to +2.5V. A reading close to +5V or 0V indicates either a fault on the Control Board, a setting error or that the source is out of calibration.

The two frequency discriminators U629 / U634-639 are not used in current products.

Programmable I/O

The section consists of an array of 24 balanced drivers and 24 balanced receivers. These can be set to interface to the back panel or disc controller as required, and route the required clock / data signals to the PLL. Data streams IOLINK[23:0] are supplied by FPGA U718. Control lines CIOI[35:0] and CIOO[51:0] are supplied by the I/O CPLD U656.

Each block of driver circuitry is the same, part of driver U704 is described here. Control line CIOO[1] is normally low to enable the outputs of latch chip U704. Data stream IOLINK[0] connects to octal latch U701 data inputs D0 &D1 and via XOR gate U703/6 to D3 &D4. Control line CIOO[5] is either high so that U703/6 inverts (for a balanced feed) or low so that U703/6 does not invert. CIOO[2 – 4] enable one of U711, 712 or 713, routing either –CLK24, -CLK22 or FCLK to the latch clock input. On the rising edge of the selected clock, data is clocked to outputs Q0-Q3, which are connected in pairs via 47R resistors R707-710 to increase current capacity. Clamp diodes D701 and 24R resistors R715-716 protect the drivers, connecting to IOC[0] & -IOC[0]. U701/7 and TR70 regulate the supply to U704 to either +3.3V or +5V under the control of CIOO[0].

Each block of receiver circuitry is the same, part of U706 is described here. A balanced data or clock stream IOC[1] / -IOC[1] connects to the differential inputs of receiver U706/3. IOC[1] also connects to the + input of U706/13 and the – input connects to bias network R720/721, which sets the input to +1.3V (suitable for Word Clock detection). The biasing can be forced to 0V or +3V by CIOI[4], this line is usually tri-stated. Only one section of U706/3 is enabled at a time by CIOI[2] or CIOI[1], the outputs are connected together. Gate U737/8 connects the outputs to IOLINK[1], when CIOO[1] is high.

The I/O connections are brought out on CN82 & CN83, both of which have 4 balanced inputs, 4 (nominally) balanced outputs, 4 balanced I/Os (selectable as input or output), power and ground.

RS232 interface

The RS232 transceiver consists of UART U408, U973 and RS232 interface chip U974. U975 and latching relays RL91/92 route the interface to CN34 and CN35 or link the two connectors for “loop through” when the board is inactive. This interface is primarily used for production testing but it may also be used with a home automation system.

Analogue Board interface

The large DIN41612 connector CN11 connects to the I/O board, this is most commonly a DAC Board. The connector carries power, ground, noise-shaped data buses NSDATAL[5:0] & NSDATAR[5:0], clocks and the RDY strobe. FPGA U505 generates the NSDATA and strobe line FRDY, which is re-clocked by latch U655 and buffered by U654.

The Display Board connects via CN16 in the lower right corner.

Header CN22 connects to the high-speed interface board (IEEE1394 and / or USB).

Drawings

Circuit diagram file: 156540cd7j3.pdf
Component layout file: 156540cl7j.pdf

The functionality of this board can be completely changed by loading different software, so it is not practical to draw a general block diagram. Refer to the Service Manual for the specific product.

HARDWARE HISTORY

The version 7 Control board was introduced on the P8i Player and Verdi Encore Transport in 2005. A few years later, the imposition of the RoHS Directive (which bans lead and certain other heavy metals from manufactured products) necessitated a re-design of the electronics used in all dCS products, bringing production of the “Classic” range (Elgar, Verdi, etc.) to an end and prompting the launch of Scarlatti, Paganini and Puccini.

The v7 control Board has been steadily updated to improve reliability and accommodate new product designs. The various modification states are identified by a 3-character issue code such as **7g5**, each state is supported by a dCS Modification Note.

The Control Board build versions used on the current product range to date are as follows:

	7g2	7g3	7g4	7g5	7j3
Scarlatti Transport	✓	✓	✓		✓
Scarlatti DAC	✓	✓	✓		✓
Scarlatti Clock		✓	✓	✓	✓
Scarlatti Upsampler				✓	✓
Paganini Transport		✓	✓		✓
Paganini DAC		✓	✓		✓
Paganini Clock			✓		✓
Paganini Upsampler					✓
Puccini Player		✓	✓		✓

Do not swap Control Boards between different models, as some builds / variants will not work correctly in all products. Consult dCS before considering replacing a Control Board.

The Modification Notes listed below describe these build states, they are available on request.

156540mn20 Updates version 7g2 to 7g3

Modification: add a wire link to the back of the board to suit the Scarlatti Clock.
All Scarlatti Clocks were built with version 7g3 or later, so it should not be necessary to perform this modification in the field.

156540mn22 Updates version 7g3 to 7g4

Modification: cut a track on the back of the board and fit a 560 ohm leaded resistor, as described on the mod note.
A hardware bug in version 7g2 and 7g3 occasionally prevents the VP3 & V1P8 power rail (and several others) turning on at power up, so that the unit fails to boot up. This modification ensures the power rails work correctly. The bug is rare (around 1% of boards were affected), so it is not necessary to modify 7g2 / 7g3 boards unless this fault occurs.

156540mn26 Updates version 7g4 to 7g5

Modification: add a wire link to the back of the board to suit the Scarlatti Upsampler.
All Scarlatti Upsamplers were built with version 7g5 or later, so it should not be necessary to perform this modification in the field.

These modifications were combined into a board update, this was released as version 7j3.

PRODUCT-SPECIFIC VARIANTS

Minor changes are needed to the Control Board to suit some products, these are:

Scarlatti DAC

Most dCS products use one mains transformer but the **Scarlatti DAC** uses 2 mains transformers connected to CN17 & CN18. The snap-off tab between connectors CN17 & CN18 must be removed if a new Control Board is fitted to a **Scarlatti DAC** – this separates the digital and analogue power supplies as intended.

Scarlatti Transport, **Paganini Transport, Puccini Player**

Transports and Players using an Esoteric CD mechanism require a 27MHz crystal oscillator (XTL0034270) to be fitted in position X03. The frequency of this crystal is locked to the frequency of X02 (22.5792MHz) using the secondary PLL.

Scarlatti Clock, Paganini Clock

Clocks have a temperature stabiliser block fitted over the crystal oscillators. These two models are calibrated in an environmental chamber during production, at which point a table of temperature-compensation data is loaded into the Control Board's flash memory. If it is necessary to replace the Control Board in one of these units, make sure the replacement board has been calibrated as a Master Clock at dCS. Fitting an un-calibrated board to a Master Clock results in large frequency errors.

Master-Mode Calibration

Control Boards in all Transports, Players, DACs and Upsamplers are calibrated during production so that they will generate a reasonably accurate clock frequency when operated in Master Mode. This involves adjusting the clock frequency to within +/-1ppm of the standard frequency at one spot temperature only. Note that the resonant frequency of a crystal oscillator drifts with temperature and these models do not correct for such drift. At running temperature, the crystal frequency can drift from this calibrated setting by around +/-10ppm, this does not affect normal operation.

KNOWN FAULTS & FIXES

Verify the fault and then check the issue of software that is loaded. If updated software is available, load it and then re-check that the fault is still present.

Symptom: A Transport or Player boots up but the CD mechanism is unresponsive or runs at the wrong speed.

- This intermittent fault is often caused by failure of the 27MHz crystal oscillator, X003. Replace it.
- Soldering faults around U606/U607 or failure of one of these chips can also cause this fault.
- Check for a faulty clock connection to the Esoteric CD mechanism.

Symptom: The unit fails to power up, the VP3 and VP5 power rails are present.

- Use an oscilloscope to check that a stable 22.579MHz clock is present at the microcontroller, U402 pin 5. If it is unstable in frequency or missing, replace crystal oscillator X002 and re-check.

Symptom: The unit powers up correctly but fails to lock to 48kHz-related data streams.

- Check that this is not caused by a mismatch of Word Clock and data sample rate. For example, a DAC cannot lock to a 44.1kHz Word Clock while receiving data at 32, 48, 96 or 192kS/s.
- The most common cause of locking problems at 32, 48, 96 or 192kS/s or freezing when changing to one of these rates is failure of the 24.576MHz crystal oscillator, X001. Replace X001 and re-test.

Symptom: The unit fails to lock and behaves inconsistently.

- Check for soldering faults in the PLL section or around U606/U607.
- Failure of U606/U607 can cause similar symptoms.

Symptom: The unit fails to power up, there are burned power supply components.

- If the PCB surface or tracks have been damaged, it is unlikely that the board can be repaired. Take a digital photo of the damage and send it to dCS with the unit serial number to request assistance.
- If the PCB surface or tracks are intact, it is possible that the board can be repaired at dCS. Take a digital photo of the damage and send it to dCS with the unit serial number to request Control Board repair.

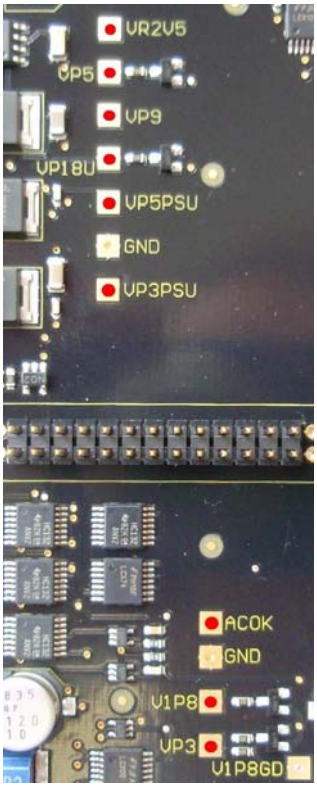
Symptom: The unit fails to power up, some power rails are turned off.

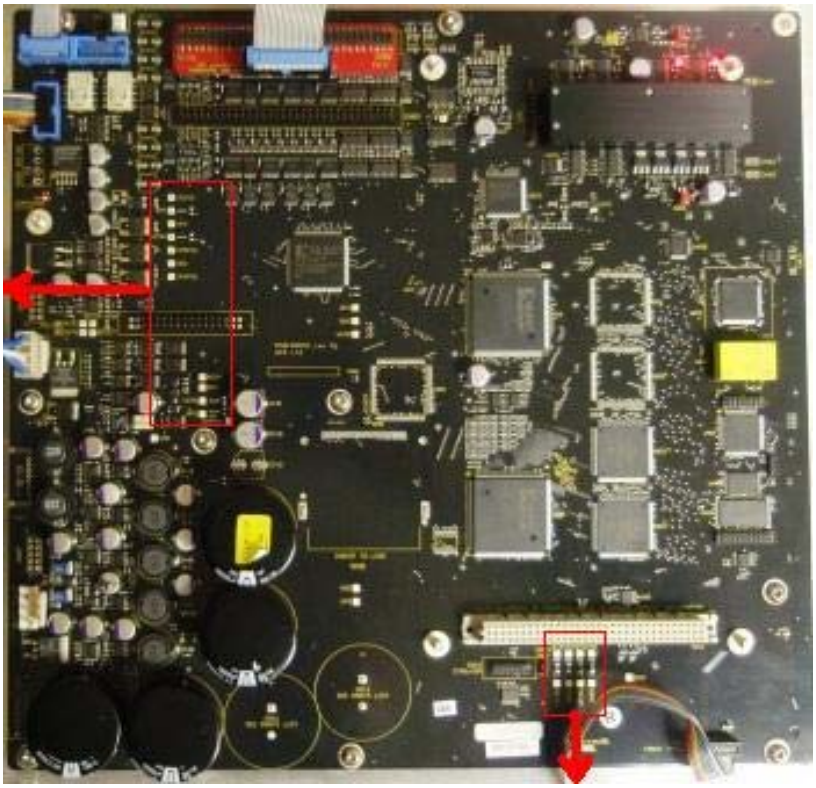
- If the Control Board version is version 7g2 or 7g3 and power rails VP12, VP3PSU3, VP5PSU, VP9 & VR2V5 are present but VP3, V1P8 and the other rails are not, this is a known (but rare) hardware bug. Modify the board as detailed in modification note 156540mn22, available from dCS on request.

FAULT-FINDING GUIDE

Symptom: The unit fails to power up

- Is low voltage AC reaching Control Board at connectors CN17 / CN18? With nominal mains voltage, the AC voltage (referred to the base plate) at pins 1 & 4 (blue wires) should be 10V rms and at pin 2 (white wire) should be 0V. If the voltage is substantially different, check the transformers for signs of overheating.
- To check the Control Board Power Supply circuitry, measure the DC voltages between GND (or the base plate) and the various square test point pads shown as red dots on the pictures below. You may will need to lift the 1394 main board and DAC Analogue Board clear to do this (switch off the power first!).

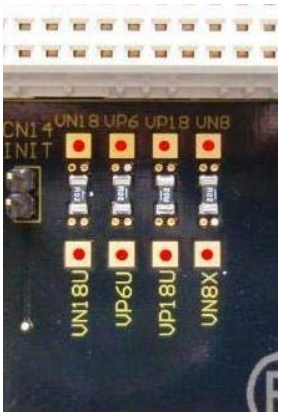




After the unit has booted up, typical measurements are:

Name	DC Voltage
VR2V5	+2.500V
VP5	+5.0V
VP9	+8.5V
VP18U	+17.8V
VP5PSU	+5.0V
VP3PSU	+3.4V
ACOK	+3.4V
V1P8	+1.78V
VP3	+3.4V

Name	DC Voltage
VN18	-18.6V *
VN18U	-18.6V *
VP6	+6.5V
VP6U	+6.5V
VP18	+17.8V
VP18U	+17.8V
VN8	-5.8V
VN8X	-5.8V



* In the Scarlatti DAC, the Paganini DAC and the Puccini Player, the VN18U power rail is disabled at initial switch-on and will not measure -18V until the unit has successfully booted up. Transports, Upsamplers and Clocks do not use the VN18U power rail and it remains permanently disabled.

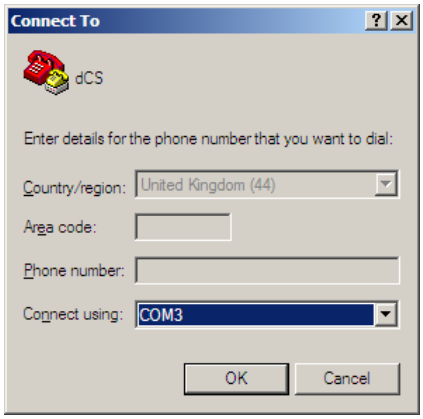
If any of these measurements are different by more than 5%, this indicates a fault in the power supply or that the power supply is being overloaded by the circuitry it is supplying. Power down, disconnect the 1394 Board and DAC Analogue Board, then power up and check to see if this has corrected the voltages.

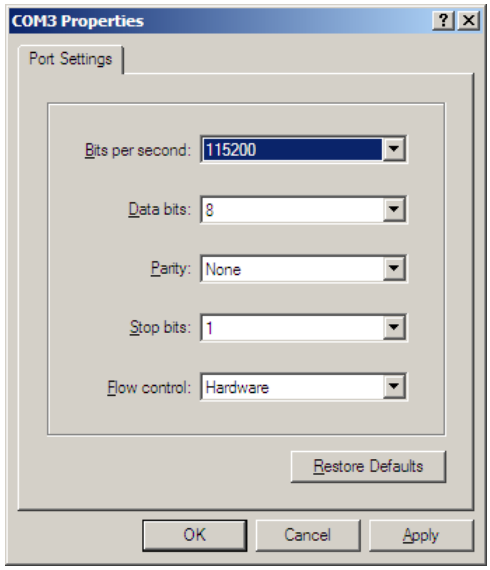
- If power is reaching the Control Board, check the behaviour of the red diagnostic LED D401, located near the front right corner of the Control Board. When power is applied, the LED should flash once and then flash twice a few seconds later. It should remain off for about 20 seconds while the board boots up, then turn on. If this does not happen but there is some LED activity, the software may have been corrupted. Try re-loading the software from ROM, as described on page **15**.
- If necessary, detach the DAC Analogue Board from the Control Board and move it out of the way. At the back right corner of the Control Board, you will see 2 metal-cased crystal oscillators X001 & X002. There is provision for 4 crystals on the board, a red LED behind each turns on when the crystal is powered. At power up, the LED behind X002 should turn on and stay on. During boot-up, the LEDs behind the other 3 crystal positions should flash together on 2 occasions. Check that a 22.6MHz clock appears at U626 pins 3 & 4. If not, X002 or U613 may be faulty.

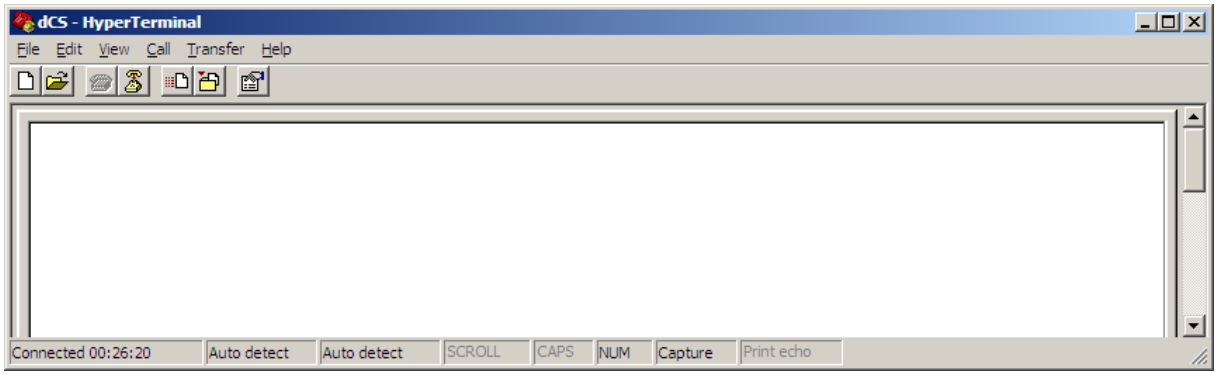
Symptom: The unit powers up but does not run correctly.

If the Control Board microcontroller is running, the diagnostic connector CN12 (located at the right side of the board) may be connected to the RS232 port of a PC running Hyperterminal (hypertrm.exe) to extract diagnostic information from the Control Board. Hyperterminal is an accessory program supplied with Windows. A suitable **RS232 to TTL** adapter cable is available from AVIT Research (www.avitresearch.co.uk) and other suppliers.

- Connect the cable between the PC port and CN12.
- Run hypertrm.exe.
- Enter a suitable name (e.g. **dCS**) and click **OK**.
- Select the serial port you are using from the drop-down box (**COM3** is used in the example below) and click **OK**.
- Set up the **Port Settings** panel as shown below and click **OK**.
- In the HyperTerminal window, click on **Transfer** / **Capture Text...**, specify a location for the text report and click **Start**.







When you power up the dCS unit, text should appear rapidly in the HyperTerminal window.

- Once the unit has booted-up and the flow of text has stopped, press the front panel buttons. The flow of text will start up again, briefly. Make sure you do not leave the unit is Standby mode.
- For a DAC, Upsampler or Player, connect a 44.1kS/s source to the selected input. For a Transport, connect a 44.1kHz Word Clock to the W/Clk Input. More text will appear.
- Change the digital source rate to 48kS/s or the Clock frequency to 48kHz. More text will appear.
- Click on **Transfer** / **Capture Text** / **Stop**.
- Disconnect the unit from the PC.

You can inspect the file using Notepad or a word processor. The file “PDC diagnostic report.pdf” is a typical report generated by a working Paganini DAC. Comments are highlighted in yellow. Note that other dCS models may not be fitted with a DAC board or a 1394 interface, so their reports will be different. Comparing the two files may indicate a fault in the unit under test, for example a stuck button or a locking problem.

dCS Service Department have a diagnostic system that performs an extensive test of the Control Board functions. This is the best way to diagnose Control Board faults.

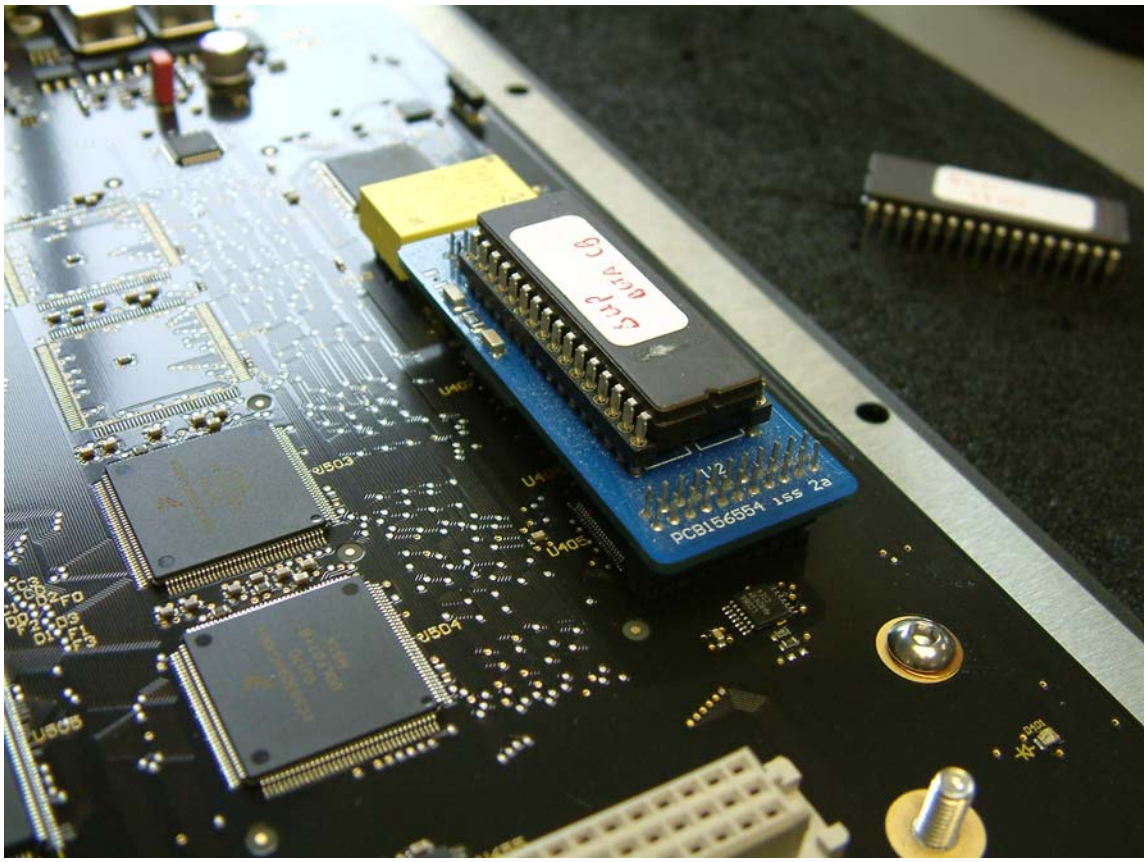
RE-LOADING SOFTWARE FROM ROM

Normally, software can be updated from CD without opening the unit case, provided the unit boots up and runs correctly.

Occasionally, the software stored in the flash memory becomes corrupt, usually as a result of a power failure or user error while CD Updating. There is also some evidence that nearby electrical storms can do this. If the software has become corrupt, it is necessary to reload the unit from a ROM. To do this, you will need a DCS156554 programmer board and a ROM which is loaded with software to match the model. You can load an older version from ROM and then CD Update to the current version if necessary.

- Power the unit up and then pull out the power cable.
- Open the case and disconnect the Display Board ribbon cable (if necessary).
- If the unit is a DAC, remove the 4 screws securing the DAC Analogue Board and pull it off the Control Board.
- Fit the appropriate ROM to the socket in the programmer board, ensuring that the notched end is beside the “U2” label. The example shown below is a Scarlatti DAC v1.01 ROM.

- Fit the programmer board onto the 3 headers near the edge of the Control Board, as shown below, making sure all pins fit into the sockets on the underside of the programmer board.



- Connect the power cable.

The Control Board will power up, red LED D401 will flash once and LEDs elsewhere on the board will turn on. The loading process takes several minutes, please be patient. When it is complete, the red LED D401 will start flashing steadily.

If D401 is still off after more than 10 minutes, the software has failed to load for some reason. Pull out the power cable, make quite sure the programmer board and ROM are correctly seated and repeat the process.

- Disconnect the power cable.
- Remove the programmer board and ROM, put them somewhere safe in anti-static packaging.
- If the unit is a DAC, fit the DAC Analogue Board on the Control Board and secure it with the 4 screws.
- Reassemble the unit, remembering to connect the Display Board cable (if it was disconnected earlier).
- Open the menu and check that on the **Information** / **Version Information** page, the **Control version** matches the ROM issue.
- Check that the unit is operating correctly.